



# Module (Course Syllabus) Catalogue

## 2024-2025

College/ Institute	Technical College of Computer and Informatics Engineering				
Department	Artificial Intelligence and Robotic Engineering				
Module Name	Digital Logic Design				
Module Code	DLD202				
Semester	2				
Credits	5				
Module type	Prerequisite Core X Optional				
Weekly hours	Four hours				
Weekly hours (Theory)	( 2 )hr Class ( 2 )hr Workload				
Weekly hours (Practical)	( 2 )hr Class ( 2 )hr Workload				
Lecturer (Theory)	Zardasht Abdulaziz Abdulkarim SHWANY				
E-Mail & Mobile NO.	zardasht.abdulkarim@epu.edu.iq, 07504612522				
Lecturer (Practical)	Karwan Hoshyar Khoshnaw				
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ECTS Workload Calculation Form Digital Logic Design Course						
S	Activity	Description	Activity Type	No Time Factor		Workload
1	Course	Theory In Class	Face to face activity hours	12	2	24
2	Course	Preparation Theory	Household activity hours	12	2	24
3	Course	Practical	Face to face activity hours	12	2	24
4	Course	Preparation Practical	Household activity hours	12	2	24
5	Assignment	Homework	Household activity hours	2	4	8
6	Assessment	Quiz	Household activity hours	2	4	8
7	Assessment	Mid Term Theory	Face to face activity hours 1		1	1
8	Assessment	Mid Term Theory Preparation	Household activity hours 1		4	4
9	Assessment	Mid Term Practical	Face to face activity hours	1	1	1
10	Assessment	Mid Term Practical preparation	Household activity hours	1	4	4
11	Assessment	Final Theory	Face to face activity hours	1	2	2
12	Assessment	Final Theory Preparation	Household activity hours	1	5	5
13	Assessment	<b>Final Practical</b>	Face to face activity hours	1	1	1
14	Assessment	Final Practical preparation	Household activity hours <b>1</b>		5	5
			Face to face huors/12 week	4.42	F. to F. huors	53
			Home huors/16 week	5.13	Home huors	82
			Total huors/20 week	8.44	Total huors	135
			ECTS ( Total hours / 27 )	5	Accepted	

## **Course Book**

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Course Description	This course will give principals of the Digital logic design with all the fundamentals of Digital logics in such a way that they will gain theoretical and practical experience of about the fundamental concepts of Digital logic design including Logic Gates, Boolean Algebra Theorem, Universal Gates, Adders, Subtractions & Flip Flops, and design Digital Logics.			
Course objectives	<ul> <li>After taking this course, students have ability to:</li> <li>1-Providing a comprehensive understanding of the main principles of digital logic design.</li> <li>2- Clarify the main digital laws.</li> <li>3- Apply these principals practically.</li> </ul>			
Student's obligation	<ol> <li>Class attendance is important, and attendance will be taken every lecture.</li> <li>The student submits a weekly report about what have done in the Lab section. For examination, there are semester exam and final exam for the practical and the theory parts. During the class hours there will be some quizzes</li> </ol>			
Required Learning Materials	Smartboard, White board, and projector.			
Assessment scheme	<ul> <li>15% Midterm Practical</li> <li>10% Midterm Theory</li> <li>8% Quiz</li> <li>5% Assignment (homework)</li> <li>40% Final Practical</li> <li>20% Final Theory</li> </ul>			
Specific learning outcome:By the end of the course, students should be able to: 1. Recognize different numbering systems. 2. Convert numbers from system to other. 3. Execute binary arithmetic.				

	truth table. 5. Convert any logic equation into logic circuit.				
	6. Minimize logic equation to get minimized logic circuit.				
	7. Implement any logic circuit using one type of logic gates either NOR				
	or NAND gates.				
	8. Use logic modules (Adder, decoder, multiplexer, demultiplexer).				
	9. Recognize different types of flip flops and convert one type into				
	another.				
	10. Implement registers using flip-flop.				
	1.Godse, Atul P., and Deepali A. Godse. Digital Logic Design &				
	applications. Technical Publications,				
	2. Digital Logic Design, Brian Holdsworth, Clive Woods.				
Course References:	3. Brown, Stephen D. Fundamentals of digital logic with Verilog				
	design. Tata McGraw-Hill Education.				
	design. Tata McGraw-Hill Educati	on.			
	4. Digital Design: A Systems Appro				
	4. Digital Design: A Systems Appro	oach, William Jai	mes Dally (Author),		
	4. Digital Design: A Systems Appro R. Curtis Harting.	oach, William Jai	mes Dally (Author),		
Course topics (Theor	<ul> <li>4. Digital Design: A Systems Appro</li> <li>R. Curtis Harting.</li> <li>5- Fundamentals of digital Logics</li> <li>6- Internet recourses.</li> </ul>	oach, William Jai	mes Dally (Author),		
Course topics (Theorem Introduction to Digital Lo	<ul> <li>4. Digital Design: A Systems Appro</li> <li>R. Curtis Harting.</li> <li>5- Fundamentals of digital Logics</li> <li>6- Internet recourses.</li> </ul>	oach, William Jai by A. ANAND KU	mes Dally (Author), IMAR Learning		

Introduction to Digital Logic	1	
Numbering systems (Decimal, Binary, Octal, and	2	1, 2
Hexadecimal). Number base Conversions.		
Conversion: Decimal Number, Binary Number,	3	1, 2
Conversion: Octal Number, Hexadecimal Number.		
Binary Arithmetic: Addition. Subtraction: 1st complement, 2nd Complement	4	3
Logic Gates (NOT, AND, OR, NAND, NOR).	5	4
Exclusive-OR (EX-OR), Exclusive-NOR (EX-NOR),		
Universal Gates (NAND Gate + NOR Gate).	6	4, 7

Rules in Boolean Algebra.	7	8
De- Morgan's Theorems.	8	8
Logic expression and truth table of a logic circuit.	9	8
Combination Logic Sum of Products and Product of Sum.		
Adders (Half Adder /Full Adder). Subtractors (Half	10	8
Subtractor/ Full Subtractor). Comparator		
Minimization With Karnaugh Maps,	11	6
Decoders, Multiplexers, Demultiplexer	12	8
Flip-Flops (RS Flip-Flop), (Clocked RS Flip-Flop). (J-K Flip-	13	9, 10
Flop), (D Flip-flop), (T Flip-Flop).		
Practical Topics	Week	Learning Outcome
NOT, OR, AND gates using ics	1	4
NOR & NAND gates using ics	2	4
Ex. Or gate and Ex. NOR gate.	3	5
De morgan's theorems	4	7
Universal gates.	5	7
Half-adder and Full-adder.	6	8
Half-subtractor and Full-subtractor	7	8
Comparator.	8	8
Seven-Segment display.	9	8,9 and 10
Decoder	10	8,9 and 10
Up counter. Down counter	11	8,9 and 10
Clock Generation by Integrate Logic (IC 555)	12	8,9 and 10

### **Questions Example:**

Ministry of Higher Educ & Scientific Researc Erbil Polytechnic Unive Technical College of Cor and Informatics Engine Al and RE Departme	ch ersity nputer eering	Final Exa	EPU EPU em: (Secon	d Semeste	er)	Class: First Module Name: Digit Module Code: DLD2 Time: 120 Minute Date: 6/6/2025	
Q1/ a) Convert the fo	ollowing Nu	mbers b	pelow:				(30 Mark)
1- Hex. Number	(7AF) 16 to C	Octal Ni	umber.				
2- Binary Numbe				l Numbe	er.		
b) Make a truth ta	able for com	nparing	two Bit	number	s.		
Q2/ Find the result for	the following	g operat	ion using	g (Full-A	dder) ar	d draw it:	(20 Mark)
	1111						
	<u> 1011 -</u>						
Q3/ Simplify a Karnau	gh map shov	vn belov	v write th	ne Boolea	an Expre	ssion and draw it.	(25 Mark)
		00	01	11	10		
	AB						
	00	1	1	0	1		
	01	0	0	1	1		
	11	0	0	1	1		
	10	1	1	0	0		
Q4/ Answer the F	ollowing:						(25 Mark)
a) What are the ty	nes of mult	ivibrato	nrs?				
b) Draw the logic	-			with tim	ing diag	ram.	
	-		- • <b>·</b> ·		- 0	Lecture	er
						Zardasht Abdulazi	z Adaulkarım

**Extra notes:** I feel we need to spend more time; we will not have enough time to go through the topics in detail, it will be better to increase the theoretical hours to make more imagination about this subject.

#### **External Evaluator**