Module (Course Syllabus) Catalogue

2022-2023

College/ Institute	**Khabat Technical Institute**
Department	**Information Technology**
Module Name	**Computer Organization and Logic Designs**
Module Code	**COL105**
Degree	**Technical Diploma** ☐ **Bachler** ☐ **High Diploma** ☐ **Master** ☐ **PhD** ☐
Semester	**1st**
Qualification	**MSc**
Scientific Title	**Assistant Lecturer**
ECTS (Credits)	**6**
Module type	**Prerequisite** ☐ **Core** ☐ **Assist.** ☐
Weekly hours	**4**
Weekly hours (Theory)	**(2)hr Class** **(55)Total hrs Workload**
Weekly hours (Practical)	**(2)hr Class** **(95)Total hrs Workload**
Number of Weeks	**11**
Lecturer (Theory)	**Sozan Sulaiman Maghdid**
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Lecturer (Practical)	**Akil Khabat Radi**
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Websites	**https://epu.edu.iq**

Course Book

Course Description	Computer Architecture and Organisation is the study of internal working, structuring and implementation of a computer system. Architecture in computer system, same as anywhere else, refers to the externally visual attributes of the system. Externally visual attributes, here in computer science, mean the way a system is visible to the logic of programs (not the human eyes!). Organisation of computer system is the way of practical implementation which results in realization of architectural specifications of a computer system.
Course objectives	The course covers the basic principles of computer organization, operation and performance. It also deals with embedded systems, peripheral devices, memory management, and processor family evolution patterns. The course discusses the role of pipelining and multiple functional units in processor design. Additional there are some main objects related to studying this course: • To become familiar in following topics: ▪ How Computer Systems work & its basic principles ▪ How to analyse the system performance. ▪ Concepts behind advanced pipelining techniques. ▪ The current state of art in memory system design ▪ How I/O devices are being accessed and its principles. • To provide the knowledge on Instruction Level Parallelism To impart the knowledge on Nano programming
Student's obligation	Methods of Instruction: Methods will include lectures and demonstrations that discuss key terms, concepts and formulae of the assigned chapter. During the lecture a quiz about the basic concepts of each chapter will be given. The student is expected to read one chapter and solve the assigned problems each week. This will require an average of three hours of study outside of the classroom each week. The previously assigned problems will be collected for grading and the solutions will be derived in class. This process is designed to help the student thoroughly understand the concepts and applications of the material covered. • Attendance Procedure: Attendance will be taken at the beginning of each class. Students are expected to attend every class. Students are responsible for all material covered during any absence and assignments must be completed by the due date for credit. The absence of four or more lectures results in an involuntary withdrawal grade. Missed exams will require proof of extenuating circumstances for any make-up consideration.
Required Learning Materials	• Projector • White board • Power Point Presentation • Scientific Debate

	Work Group				
Evaluation	**Task**		**Weight (Marks)**	**Due Week**	**Relevant Learning Outcome**
	Paper Review		0		
	Assignments	Homework	5		
		Class Activity	2		
		Report	10		
		Seminar	10		
		Essay	0		
		Projects	0		
	Quiz		8		
	Lab.		10		
	Midterm Exam (T)		10		
	Midterm Exam (P)		15		
	Final Exam (T)		10		
	Final Exam (P)		15		
	Total		100		
Specific learning outcome:	✓ To introduce basic principles of computer organization and architecture. ✓ To provide examples of different processors and instruction sets. ✓ To give a basis for understanding issues of computer operation and performance. ✓ To familiarize the students with computer arithmetic. ✓ To apply the knowledge of performance metrics to find the performance of systems. ✓ To create an assembly language program to program a microprocessor system. ✓ To design a hardware component for an embedded system ✓ To deal with different types of computers ✓ To identify high performance architecture design ✓ To identify the problems in components of computer. ✓ To develop independent learning skills and be able to learn more about different computer architectures and hardware. ✓ To learn & use the new technologies in computers. ✓ To use the knowledge of micro programming in the field of speech processing.				

Course References:	**Key references:** • Weekly lecture slides • Computer Organization and Architecture, William Stallings, 5th Edition, 2000 • Digital Electronics, William Kleitz, 9th Edition
	▪ **Useful references:** • Fundamental of Digital Electronics, Barry Paton,1998 Edition • Schaum's outline of Computer Architecture, Tata McGraw Hill, 2006 ▪ **Magazines and review (internet):** • http://www.allaboutcircuits.com/textbook/digital/ • http://electronicsproject.org/ • Images for digital electronics projects using logic gates http://en.mcqslearn.com/cs/dld/digital-logic-design-mcqs.ph

Course topics (Theory)	Week	Learning Outcome
Introduction to Computer Organization & Architecture	1	• Why Study Computer Organization& Architecture • Brief History about computer • Computer Generation
Number System	2,3	• Introduction to number System • Conversion among numbering System • Arithmetic operation of binary number system
Digital System	4,5	• Introduction to Digital System • Logic gates • Boolean algebra • Simplification Techniques
Karnaugh Maps	6	• Introduction • Rules of Simplification • Examples
Digital Circuits	7	• Combination circuits • Adder & Subtraction • Decoder & Multiplexers
Continue…Digital Circuits	8	• Sequential Circuits • Flip-Flops • Register & Counters • Memory organization and storage system
Assembly Language	9	• Introduction • ASCII code • Conversion text • Addressing data items in memory

Computer Architecture The VON NEUMANN MODEL	10	Functional unit Input Unit Memory Unit Arithmetic & Logic Unit (ALU) Output Unit Control Unit
Basic Operational Concept	11	Introduction Bus Instruction

CPU		Data Bus, Address Bus & Control Bus ○ Introduction ○ Characteristic Study & Process ○ 8086 Microprocessor study in details ○ Introduction ○ Cache Memory

Practical Topics	**Week**	**Learning Outcome**
Registers and counters.	1,2	Registers and counters
Program Debugging instruction – Trace commands.	3,4	Trace commands.
Data Movement Instructions – MOV PUSH/POP	5	MOV PUSH/POP
Arithmetic Instructions – ADD/ADC/INC SUB/SBB/DEC MUL/IMUL DIV/IDIV.	6	Arithmetic Instructions
Logical Instructions – AND/OR/XOR/NOT/Test and bit test.	7,8	Logical Instructions
String Primitive Instructions.	9	String Primitive Instructions
Program Control Instructions CALL/RET/JMP Conditional Jump.	10	Program Control Instructions
I/O Instructions - IN and OUT Interrupt Instructions – INT.	11	Interrupt Instructions – INT.

Questions Example Design

1. Compositional:

Q/ Simplify this Boolean function to a minimum number of literals. $F = (A + B).(A + \bar{B})$

Solution:

$$\begin{aligned}(A + B).(A + \bar{B}) &= A.A + A.B + A.\bar{B} + B.\bar{B} \\ &= A + A.B + A.\bar{B} + 0 \\ &= A.(1 + B + \bar{B}) \\ &= A.(1 + \bar{B}) \\ &= A.1 \\ &= A\end{aligned}$$

Q/ Convert the decimal number (112.7) to:

1- Binary number

2- Octal number

3- Hexadecimal number

Solution:

1- Converting to Binary Number

a) Real Part

Dec No.÷2	Result	Remainder
112÷2	56	0
56÷2	28	0
28÷2	14	0
14÷2	7	0
7÷2	3	1
3÷2	1	1
1÷2	0	1

b) Fraction Part

Dec No.×2	Result	Carry
0.7×2	1.4	1
0.4×2	0.8	0
0.8×2	1.6	1
0.6×2	1.2	1
.	.	.
.	.	.
.	.	.

$(112.7)_{10} = (1110000.1011)_2$

2- Converting to Octal Number

a) Real Part

Dec No.÷8	Result	Remainder
112÷8	14	0
14÷8	1	6
1÷8	0	1

b) Fraction Part

Dec No.×8	Result	Carry
0.7×8	5.6	5
0.6×8	4.8	4
0.8×8	6.4	6
0.4×8	3.2	3
.	.	.
.	.	.

$(112.7)_{10} = (160.5463)_8$

3- Converting to Hexadecimal Number

a) Real Part

Dec No.÷16	Result	Remainder
112÷16	7	0
7÷16	0	7

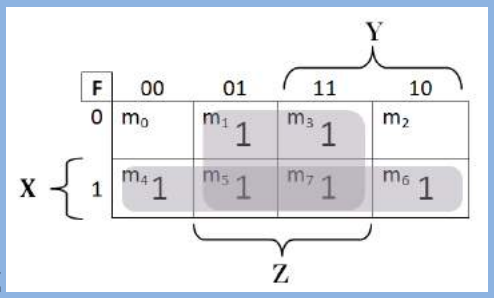
b) Fraction Part

Dec No.×16	Result	Carry
0.7×16	11.2	11=B
0.2×16	3.2	3
0.2×16	3.2	3
.	.	.
.	.	.

$(112.7)_{10} = (70.B33)_8$

Q/ Simplify the following Boolean expression function by using Karnaugh Map: $F = \sum(1,3,4,5,6,7)$

Solution:



Final Solution: **F= X+Z**

2. True or false type of exams:

1- The Boolean expression for a tow input AND gate equal to($F = \overline{A}B$). **(True)**

2- Slide Rule is inventoried by John Napier.**(False)**

3- The Full adder is a combinational circuit that performs the addition of two bits. (False)

4- A Registers holds a single bit of memory. **(True)**

5- First Electronic digital computer, was called (Mark1), build in 1964. **(False)**

6- Keyboard for input and monitor for output, first time used in 3rd generation. **(True)**

3. Multiple choices:

1- Slide Rule is inventoried by_____.

a. John Napier

b. William Oughtred

c. Ada Lovelace

d. George BOOLE

2- The Main Memory_____is used in the 2nd generation.

a. Punched Card

b. PROM & DRAM

c. RAM & ROM

d. EPROM & SRAM

3- Major Innovation using to designed computer in the 3rd generation, it's_____.

a. Transistors

b. Integrated circuit

c. Vacuum Tubes

d. LSIC and VLSIC

4- This Binary number (10101010101101111.11) is equal to_____Hexadecimal number.

a. EA378.C

b. 352158.3

c. 1D46F.C

d. 1556F.C

5- _____that is the mathematics of variables with values that can be only "True" or "False".

a) Boolean Logic

b) ENIAC

c) ABACUS

d) Pascal Machine

Extra notes:

all lectures should mostly focus on practical session because students will better learn practically, and rather than exam paper should lectures give higher mark for practical exam or practical work such as projects or practical homework.

External Evaluator

I have been reviewed this course book, its perfect and feet for this subject in the level of institute student, so I have no suggestion.

Karwan Hamasaeed Hamasharef

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