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Short communication

A Bayesian Neural Network-based approach for multistate reliability assessment of solder joints exposed to various failure mechanisms

Yongxin Li [a], Shavan Askar [b c], Soledad Paucar-Sullca [d], José-Manuel Burga-Falla [e], Renas Rajab Asaad [f]

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Highlights

- Ability to account for multiple failure mechanisms in the solder joint.
- Utilizing a Bayesian Neural Network tool to dynamically define degradation states.
- Delivering higher precise reliability assessment compared to conventional methods.

Abstract

The evaluation of the operational lifespan of solder joints in electronic devices, especially when subjected to intricate mission profiles, stands as a pivotal imperative in the domain of electronic material design. In response to this critical concern, this study introduces an innovative methodology designed to discern between gradual and sudden failures, offering a nuanced exploration of the distinct failure mechanisms at play. Distinguishing itself through a sophisticated treatment of failure mechanisms—specifically, the incorporation of thermomechanical fatigue and vibration-induced mechanisms—within the context of solder joint degradation, the proposed approach significantly elevates the precision and accuracy of reliability evaluations. This refined methodology emerges as a valuable contribution to the field, promising more insightful and reliable results in the assessment of electronic device durability under diverse and complex operational conditions.

Introduction

The evaluation and enhancement of the dependability and effectiveness of electronic systems have gained considerable traction across various industries, including automotive, aerospace, and portable devices [1]. The reliability of electronic control units, power electronics, and avionics is enhanced, contributing to the safety and dependability of vehicles and critical aerospace applications [2]. In the realm of portable devices and consumer electronics, the reliability of smartphones, laptops, and gadgets is influenced by the approach, catering to diverse usage scenarios and improving customer satisfaction [3]. The benefits, including cost savings through minimized replacements and repairs, are extended, aligning with sustainability goals by curbing electronic waste through longer-lasting components. Semiconductors, as a component within the realm of electronics, have emerged as a highly susceptible element due to increased exposure to external stresses and the inherent complexity of their structure [4]. The inquiry into failure mechanisms associated with semiconductors is methodically classified into two distinct categories, specifically designated as chip- and package-level analyses [5]. At the package level, these failure mechanisms emanate from the intricate physical structure of semiconductors, where distinct components possessing diverse material properties are intricately interconnected [6]. Predominantly documented damages at this level are encapsulated by phenomena such as solder joint void propagation and bonding wire lift-off [7,8]. Solder joint void propagation pertains to the gradual formation and propagation of voids within the solder joints, introducing vulnerabilities in the interconnection. Concurrently, bonding wire lift-off refers to the detachment of bonding wires from their intended positions, disrupting the structural integrity of the semiconductor packaging [9]. This meticulous categorization and examination of failure mechanisms at both the chip and package levels contribute to a nuanced understanding of semiconductor vulnerabilities, thereby facilitating targeted strategies for their mitigation and the enhancement of overall system robustness. Semiconductors encounter diverse and intricate mission profiles that significantly impact their performance under both ideal and imperfect conditions [10]. Understanding and analyzing the impact of complex operational scenarios on semiconductors is crucial. It involves considering various factors and parameters to identify vulnerabilities, develop robust design strategies, and ensure reliable electronic systems. Accurate characterization of semiconductor behavior under diverse mission profiles is essential for optimal performance and extended lifetime.

Thermomechanical fatigue and vibration-induced failure mechanisms have garnered considerable attention as prominent causes of semiconductor failure, greatly diminishing their operational lifetime [11]. These failure mechanisms, among the range of potential culprits, are extensively documented in the literature as primary contributors to the deterioration of semiconductor devices [12,13]. Understanding the detrimental effects of thermomechanical fatigue and vibration is vital for comprehending the mechanisms underlying semiconductor failure and devising strategies to mitigate their impact. Thermomechanical fatigue gradually degrades semiconductors, while vibrations cause sudden failures. Understanding these distinct failure mechanisms is crucial for enhancing semiconductor reliability assessment. Previous research endeavors have utilized failure modes and effects analysis (FMEA) as a means to prioritize the most significant failure mechanism in order to facilitate reliable assessments [14]. While FMEA can be appropriate for straightforward mission profiles, its limitations arise when attempting to address multiple concurrent failure mechanisms, a common occurrence in real-world applications.

This paper introduces a novel approach for comprehensive reliability evaluation that accounts for multiple failure mechanisms by classifying them into gradual and sudden categories. The proposed methodology incorporates a multistate degradation algorithm, distinguishing between gradual degradation and sudden degradation. The gradual degradation mechanism encompasses various states, including imperfect, healthy, and failure states, reflecting the progressive nature of the system's deterioration.

Section snippets

Principles of the proposed reliability approach: a comprehensive framework

In this section, the BNNRA method incorporates well-known failure mechanisms, such as thermomechanical fatigue and vibration-induced effects. Thermomechanical fatigue, characterized by gradual deviations in electronic components such as increased thermal and electrical resistances, accelerates aging and alters the operating point. Consequently, the component experiences different mission profiles from a healthy to failure state. A multistate degraded system accounts for these changes during…

Results and discussion

In this section, a case study compares the performance of the proposed algorithm with other reliability assessment methods. The study focuses on a power IGBT used in an automotive interface power converter, subjected to severe thermomechanical stresses and vibration. Two types of failure mechanisms are considered. Fig. 4 meticulously illustrates the performance metrics of the BNN model, accompanied by their respective hyper-parameters, throughout the rigorous 4-fold cross-validation process.…

Conclusion

In conclusion, the proposed Bayesian neural network reliability assessment (BNNRA) methodology considers distinct failure mechanisms and provides accurate estimations of solder joint lifetime. The comparison with other methods reveals variations in predicted lifetimes, and the calculated percentage errors highlight disparities between predicted and actual lifetimes. The optimized multistate reliability assessment, particularly the BNNRA method, plays a crucial role in material design by…

CRediT authorship contribution statement

Yongxin Li: Supervision, Validation, Visualization, Writing – review & editing. **Shavan Askar:** Writing – review & editing, Writing – original draft, Data curation, Conceptualization. **Soledad Paucar-Sullca:** Writing – original draft, Software, Resources, Investigation, Formal analysis, Conceptualization. **José-Manuel Burga-Falla:** Visualization, Validation, Software, Methodology. **Renas Rajab Asaad:** Writing – review & editing, Validation, Supervision, Project administration, Methodology,…

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.…

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References (18)

D. Teng *et al.*
Aero. Sci. Technol. (2024)

C.-P. Wang
IEEE Trans. Device Mater. Reliab. (2019)

J. Leppänen *et al.*
Microelectron. Reliab. (2021)

S. Liu *et al.*
Microelectron. Reliab. (2021)

M. Lederer *et al.*
Power electron
Devices Components (2023)

B. Gao *et al.*
Microelectron. Reliab. (2018)

N. Muhammad *et al.*
Microelectron. Reliab. (2020)

M. Ekpu *et al.*
Microelectron. Reliab. (2014)

U. Choi *et al.*
IEEE Trans. Power Electron. (2015)

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